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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,512	08/31/2001	Yasuo Osone	500.40530X00	8183

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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 11/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,512	OSONE ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25,27,46 and 47* is/are allowed.

6)☒ Claim(s) *14-24,26,28-45,48 and 49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 21, 22 and 39-42 are rejected under 35 U.S.C. 101 as being non-statutory because they improperly embrace or overlap two different statutory classes of invention, namely, manufacture and process of using the manufacture, which statutory classes are set forth only in the alternative in 35 U.S.C. 101. In particular, claims 21, 22 and 39-42 are directed to a manufacture, but the limitation, "heat dissipated from a transistor or transistors of a semiconductor substrate mounted on the multilayer wiring board substantially coincides" is directed to a process of using the manufacture.

Also claims 21, 22 and 39-42 are rejected under 35 U.S.C. 112, second paragraph, because they are directed to both manufacture and a process of using the manufacture. As a result, the scope of the claims cannot be determined. See MPEP 2173.05(p)II. Specifically, claims 21, 22 and 39-42 are directed to a manufacture, but the limitation, "heat dissipated from a transistor or transistors of a semiconductor substrate mounted on the

multilayer wiring board substantially coincides" is directed to a process of using the manufacture.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 14-20, 23, 26, 28-38, 43-45, 48 and 49 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by applicant's admitted prior art.

At page 10, lines 19-24; page 11, lines 12-17; page 12, line 1 to page 16, line 22; page 19, line 24 to page 20, line 8; page 26, lines 10-17, applicant admits as prior art the following:

A multilayer wiring board 3 having through holes 4 in a thickness-wise direction, wherein a semiconductor substrate 1 mounted on the multilayer wiring board has through holes 5 in a thickness-wise direction thereof, and wherein the through holes in the semiconductor substrate are located relative to the through holes in the multilayer wiring board so that entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas (areas including at least both 4 and 5), which the through holes in the multilayer

wiring board occupy; wherein conductive layers 6 are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material; wherein a semiconductor element 1 is mounted, in which conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material; wherein wirings 6, which connect heating areas in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate, and electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface of the multilayer wiring board, on which the semiconductor substrate is not mounted, in this order; wherein said semiconductor substrate includes emitter electrodes 7 located on a first main surface of the semiconductor substrate and a plated heat sink 6 located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board; wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate; wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer 2.

A multilayer wiring board having through holes in a thickness-wise direction, wherein a semiconductor substrate mounted on the multilayer wiring board has through holes in a thickness-wise direction thereof, and wherein the through holes in the semiconductor substrate are located relative to the through holes in the multilayer wiring board so that entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate partly overlap areas (areas including at least 4 and part of 5) which the through holes in the multilayer wiring board occupy; wherein conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material; wherein a semiconductor element is mounted, in which conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material; wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate; wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

A multilayer wiring board having a cross-plane through hole or holes, wherein an in-plane location of respective heat dissipating regions in a semiconductor substrate mounted on the multilayer wiring board is inside of a through hole or an area (the total area of the board) where through holes

are built in the multilayer wiring board; wherein conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material; wherein a semiconductor element is mounted, in which conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material; wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board; wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

A multilayer wiring board having through holes in a thickness-wise direction, wherein a semiconductor substrate mounted on the multilayer wiring board has cross-plane through holes, and heat flows one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board; wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate

and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board; wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate; wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

A multilayer wiring board, wherein a semiconductor substrate having cross-plane through holes, which are connected to emitter wirings 10 connected to emitters of heterojunction bipolar transistors and extended through the semiconductor substrate and which have conductive layers on sides thereof or inside thereof, is mounted on the multilayer wiring board, and the cross-plane through holes in the semiconductor substrate and through holes extending through the multilayer wiring board are connected (at least thermally) to each other, and wherein conductive layers are provided on sides of or inside of the connected through holes in the semiconductor substrate and the wiring board, and in-plane areas, which the through holes in the semiconductor substrate occupy, in a plane of the multilayer wiring board and of the semiconductor substrate are included in areas (areas including at least 4 and 5) which the through holes in the multilayer wiring board occupy; wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the

semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board; wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate; wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

A multilayer wiring board, wherein emitter electrodes of heterojunction bipolar transistors are arranged on a semiconductor substrate, the semiconductor substrate is mounted on a wiring board, which wiring board has cross-plane through holes, and said through holes in the wiring board have on sides or inside thereof a material of good thermal conductivity, wherein the emitter electrodes are disposed in a group electrically connected by a common emitter wiring located in a plane over the semiconductor substrate, wherein emitter electrodes in a central area of the group are located over areas (areas including at least 4 and 7) which the through holes in the wiring board occupy, and wherein first and second end emitter electrodes are respectively disposed at opposite ends of the emitter electrodes in the central area of the group to protrude from the areas which the through holes in the wiring board occupy; wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the

semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board; wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

To further clarify, the scope of the language, "areas which the through holes in the multilayer wiring board occupy" is not limited in scope to areas in which ***only*** the through holes in the board occupy. In particular, for each pair of adjacent board and substrate through holes, there are areas in which the through holes in the board occupy that are larger than areas in which only the through holes in the board occupy, and can include (but not necessarily overlap) the entire areas in which the through holes in the substrate occupy, such as areas including both the entire areas in which the through holes in the substrates occupy and the areas in which only the through holes occupy.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art.

Applicant admits as conventional a semiconductor device including a plurality of finger-shaped emitter electrodes or source electrodes, and at least one via hole which are arranged in rows in a first direction on a semiconductor substrate, wherein the emitter electrodes or the source electrodes are connected to a conductive layer formed on a back surface opposite to a surface, on which the electrodes are formed, through the via hole, and wherein said emitter electrodes or source electrodes, and the via holes are arranged in parallel in a second direction orthogonal to the first direction, and the via holes are positionally shifted (in the second direction) from one another in adjacent rows among said rows.

However, applicant does not appear to explicitly admit as prior art that the rows comprising emitter electrodes or source electrodes and the via holes are arranged in parallel in a second direction orthogonal to the first direction.

Nonetheless, as reasoned from well established legal precedent, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to arrange the rows of the admitted prior art as claimed because applicant has not disclosed that, in view of the applied prior art, the arrangement is for any purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another arrangement. In fact, the only disclosure of this arrangement is in the claims. Moreover, it has been held that limitations directed to rearrangement of parts are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. In re Japikse 86 USPQ 70 (CCPA 1950); for example, reversal of parts was held to have been obvious. In re Gazda 104 USPQ 400 (CCPA 1955). Moreover, "simple adjustment of spatial orientation" has been held to be obvious. Colt Industries Operating Corp. v. Index Werke, K.G. et al., 217 USPQ 1176 (DC 1982).

Claims 25, 27, 46 and 47 are allowed.

Applicant's amendment and remarks filed 4-10-6 have been fully considered and are treated supra and infra.

Applicant asserts, "It is respectfully submitted that, in the present instance, the rejection of claim 24 is based solely upon 'common knowledge.' MPEP 2144.03 also points out that: Official notice unsupported by documentary evidence should only be taken by the Examiner where the facts asserted to be well known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well known.' In the present instance, there has been no demonstration whatsoever that the modifications necessary to the admitted prior art to arrive at the invention defined by claim 24 are 'capable of instant and unquestionable demonstration as being well known.' . . . Accordingly, in light of the failure of the Office Action to provide any documentary evidence showing that it would be obvious to modify the arrangement of Fig. 3 and 4 to arrive at the different structure of claim 24, reconsideration and removal of the 35 USC §103 rejection of claim 24 is respectfully requested."

This assertion is respectfully deemed traversed because the rejection is not based on common knowledge or Official notice. Instead, as elucidated in the rejection, the rationale for the holding of obviousness is well established legal precedence.

Relatedly, applicant alleges, "the Office Action simply states that the applicants have failed to show any unexpected result or any criticality to the applicants different claim structure. With regard to this, the specification does, in fact, clearly define that the object of the invention is to provide a multilayer wiring board 'in which thermal resistance of radiation paths is reduced to provide an improvement in radiation effect'."

These allegations are respectfully traversed because the rejection more than simply states that applicant has failed to show any unexpected result or criticality. Furthermore, it is not necessarily maintained in the rejection that there is not clearly defined object of the invention. Rather, as elucidated in the rejection, the legal precedence relied on for rationale that limitations directed to rearrangement of parts are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will

expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR: Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
26-Oct-06